Flash Memory Technology

Navid Zeraatkar
Ferdowsi University of Mashhad
navid_zeraatkar@yahoo.com

Abstract: *This paper explains Flash Memory Technology including basic Flash cell description, principles of its Read, Write and Erase operations (especially for a NOR Flash), different technologies of Flash Memory, Multi-Level-Cell Flash and challenges in this newly-born, commonly-used memory.*

Keywords: Flash Memory, multi-level-cell.

1 Introduction

Nowadays, achieving to an ideal memory is a dream for electronics world. Every month new products comes out that cause former products to have valediction. Among all memory kinds, there is not a long time that Flash Memories have born, but in a rather short period of years they could hold a large share of memory business. Since 256Kb Flash chip emerged in 1987 [1], it had very fast advances. Now Flash Memory is made in different kinds and various densities up to 4GB by a large group of semiconductor manufacturers. In the following sections some basic information about Flash Memory Technology is represented.

2 What is Flash Memory?

Flash memory stores information on a silicon chip in a way that does not need power to maintain the information in the chip. This means that if you turn off the power to the chip, the information is retained without consuming any power. This kind of memories is called non-volatile. In addition, flash offers fast read access times and solid-state shock resistance. These characteristics are why flash is popular for applications such as storage on battery-powered devices like cellular phones, PDAs, digital cameras, memory sticks, portable media devices and so on.

Flash Memories are manufactured in different technologies like NOR stack gate, Split gate, Source-side injection NAND, DINOR, AND, etc. Some of mentioned technologies plus some other technologies are still in development and are not used for business scale.

3 Principles of Operation

In this section, physical structure of a NOR Flash Memory is explained for an example. Absolutely, basis of other Flash technologies is not much different from NOR technology.

3.1 Flash Memory Cell

Flash memory stores information in an array of transistors, called "cells", each of which traditionally stores one bit of information. Newer flash memory devices sometimes referred to as multi-level-cell devices, can store more than 1 bit per cell. Multi-level-cell technology will be described in next sections.

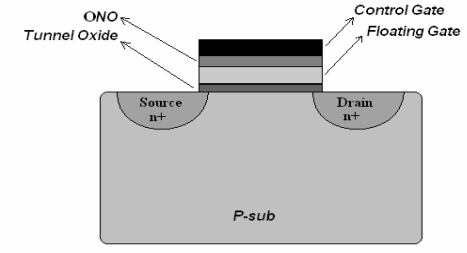

Figure 1: Flash Memory Cell

As shown in Figure 1, in NOR flash, each cell looks similar to a standard MOSFET transistor, except that it has two gates instead of just one. One gate is the control gate (CG) like in other MOS transistors, but the second is a floating gate (FG) that is insulated all around by an oxide layer. The FG is between the CG and the substrate. Because the FG is isolated by its insulating oxide layer, any electrons placed on it get trapped there and thus store the information. When electrons are on the FG, they modify (partially cancel out) the electric field coming from the CG, which modifies the transition voltage (Vt) of the cell. Thus, when the cell is "read" by placing a specific voltage on the CG, electrical current will either flow or not flow, depending on the Vt of the cell, which is controlled by the amount of electrons on the FG. This presence or absence of current is sensed and translated into 1's and 0's, reproducing the stored data. In a multi-level-cell device, which stores more than 1 bit of information per cell, the amount of current flow will be sensed, rather than simply the presence or absence of current, in order to determine the amount of electrons stored on the FG.

3.2 Write Operation

A NOR flash cell is programmed (set to a specified data value) by starting up electrons flowing from the source to the drain, then a large voltage placed on the CG provides a strong enough electric field to suck them up onto the FG. This process that even may happen in ordinary MOST is called Channel Hot Electron Injection (CHE Injection). This procedure is shown in Figure 2.

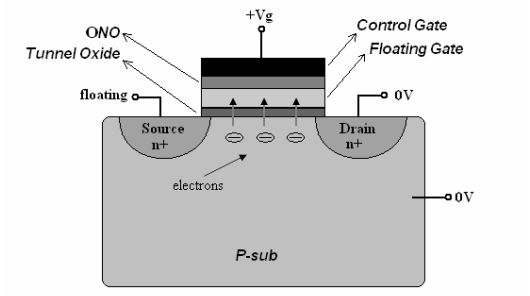

Figure 2: Write Procedure

3.3 Erase Operation

To erase (reset to all 1's, in preparation for reprogramming) a NOR flash cell, a determined voltage is placed on the substrate, while source and drain are floating and CG is connected to GND. This condition pulls the electrons off through Fowler-Nordheim tunnelling, a quantum mechanical tunnelling process. Erase procedure is shown in Figure 3.

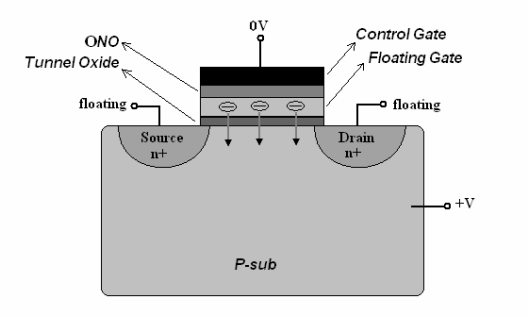

Figure 3: Erase Procedure

3.4 Read Operation

During a read operation, a high voltage is applied to the front gate. If the selected transistor is turned on, its drain output is pulled low on the Bit Line, defined as 1 using negative logic. If the selected transistor is not turned on, its drain voltage is high on the Bit Line defines as 0. Read procedure is shown in Figure 4.

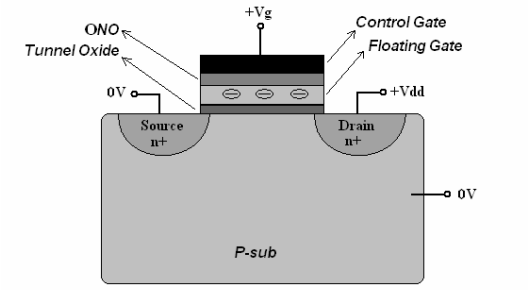

Figure 4: Read Procedure

3.5 Circuit Symbols of Cells

Circuit symbol of NOR cells is illustrated in Figure 5, where BL is Bit Line, SL is Source Line and WL is Word Line.

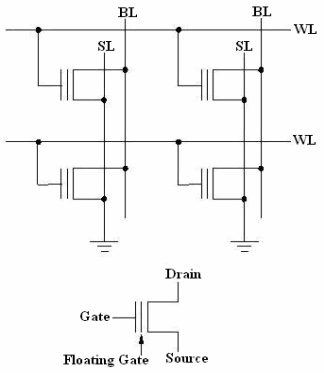

Figure 5: Circuit Symbol of Cells

4 Multi-Level-Cell Flash

According to previous sections, an ordinary Flash cell can store one bit information. As manufacturers are interested in reducing cost per bit (cost/bit) for memories, nowadays some manufacturers are developing their technology to fabricate cells which are able to store more than one bit information. This kind of cells is named "Multi-Level-Cell" (MLC). In MLC operation, the logical flash memory cell achieves for example two bits per cell using four possible states, defined by four flash cell threshold voltage ranges [2]. Each level represents an input voltage to turn on the transistor. Henceforth, each input level represents the encoding of two bits. The access time may be longer, but the capacity is doubled. If the amount of negative charge on a floating gate has eight levels, then 3 bits of information can be stored per cell. As an example a 32 Mb multilevel-cell (MLC) flash memory storing two bits of data per cell achieves 32Mb memory storage capacity using 16Mb flash memory cells. So by using this technology memory cost/bit decreases. Currently, many manufacturers use this method, like Intel Corporation that recently fabricated MLCs in 90nm technology [3].

5 Challenges and Hassles

In this section, some hassles and problems of Flash Memory whether in manufacturing process or in application are represented.

5.1 Flash and Scaling

While technology is going toward scaling down MOST due its several advantages [4], very scaled down MOSTs (deep-submicron MOSTs) can't be used for Flash cells. Deep-submicron transistors cannot tolerate the high voltages employed during the CHE (channel-hot-electron) injection and FN (Fowler-Nordheim) tunneling program and erase processes used to place charge into and remove it from the flash-memory cell's floating gate. Overload of the thin, fragile, insulating oxide layer between the floating gate and the select gate and between the floating gate and the source, drain, and substrate lead to spurious disturbance of floating-gate electrons, causing inadvertent programming or erasing. The phenomenon is particularly acute with multi-level-cell flash memories that rely on a precise amount of stored charge on the floating gate to reference a particular 2-bit value combination. This is in situation that MOS scaling technology is going ahead with an incredible speed.

5.2 Flash Wearing Out

As reputed in previous sections, during read, write and erase operations, electrons do burrow through FG insolating oxide layer in CHE injection and Fowler-Nordheim tunneling process. So several erase operations cause oxide layers to lose their specifications during the time. Consequently, after some erase operation electrons can easily and unwontedly do tunneling through oxide layer between FG and substrate. In addition, TDDB process (Time-Dependent Destructive Breakdown) of oxide layer between FG and CG that even occurs in all submicron MOSTs sharpens this problem. Hence, this phenomenon wears out Flash Memories after some erasing operation. The approximate number of allowed erasing operations is said in Flash datasheets. For example, for a NOR Flash this number is about 10,000 to 100,000 erase cycles.

5.3 Flash versus DRAM

A frequently asked question is why flash memory isn't used to replace DRAM in computers so that memory contents would not be lost when they are turned off or power is lost. The limitation of flash is that while it can be read or programmed a byte or a word at a time in a random access fashion, blocks of memory must be erased all at the same time. To explain further, flash components are generally subdivided into a number of segments called blocks. Starting with a freshly erased block, you can program any bytes within that block. However, once a byte has been programmed, it can't be changed again until it is erased, which has to be done a block at a time. In other words, flash (specifically NOR flash) offers random-access read and programming operations, but cannot offer random-access rewrite or erase operations. Thus, many applications of DRAM that involve overwriting a specific address location quickly cannot be easily implemented on flash memory. In addition, DRAM is generally cheaper than flash memory on a cost per bit basis.

6 Conclusions

In this paper Flash Memory Technology, principles of it operation and some points about its fabricating, applications and limitations was reputed.

References

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